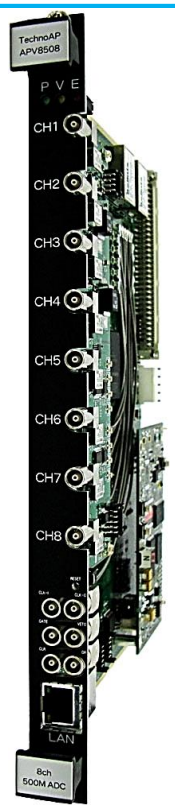
Digital Pulse Processor

TechnoAP

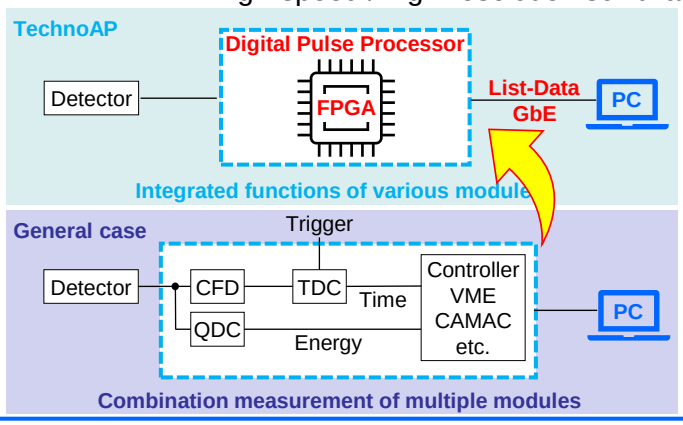
APV8508-14 500Msps, 8 ch., 14-bit VME

By adopting real-time analysis by FPGA and Gigabit Ethernet communication, high-speed processing without dead time by signal processing is realized with high time resolution and high throughput. It also supports synchronization processing between multiple boards and can be easily extended to analysis for multi-channel systems.

- Timestamp: **64-bit (Max. 55 month) 7.8 ps LSB**
- Throughput **1 Mcps and more / channel (Histogram mode)**
  150 kcps and more / 8 channels (List mode)
- Mode List (TDC + QDC etc.), Wave, Histogram, etc.
- Function (Digital) CFD, TDC, QDC, PSD **List-Wave**[*1], **Coincidence**[*1]
- Interface TCP/IP, **Gigabit Ethernet**
  Data transfer 20 M Byte/sec and more
- Use example gamma/neutron discrimination and β-ray measurement,
  high-speed / high-resolution scintillator, such as $LaBr_3$, LYSO, etc.

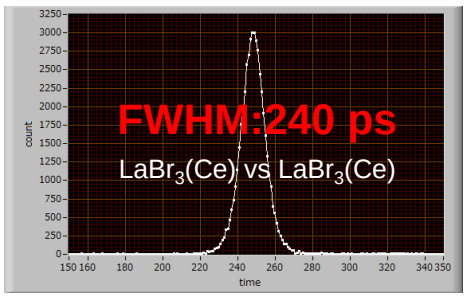


*1 Added option, Specifications modifiable.

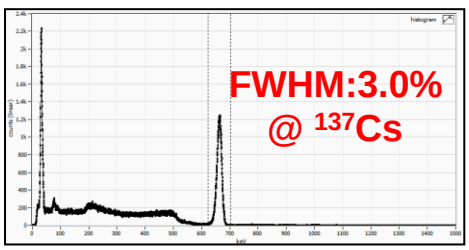


List data example (1 event : 112-bit, 14 byte)

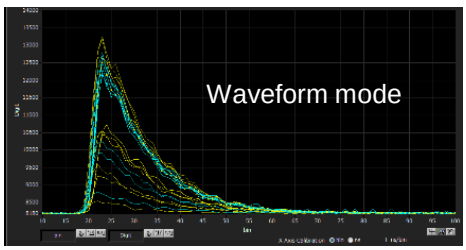
	112	96	80	16	13	0
Event#1	PSA_F[15..0]	PSA_S[15..0]	TDC[63..0]	CH#[2..0]		QDC[12..0]
Event#2	PSA_F[15..0]	PSA_S[15..0]	TDC[63..0]	CH#[2..0]		QDC[12..0]
Event#N	PSA_F[15..0]	PSA_S[15..0]	TDC[63..0]	CH#[2..0]		QDC[12..0]



Time resolution



Energy resolution



Analog signal input type	PMT anode signal, Fast-NIM signal, etc.
Analog input range	±1V, Input impedance: 50 ohm, LEMO connector
Analog gain switch	x1 / x3
Analog DC offset fix	±1V
Analog signal risetime	2 ns or less
Digital CFD	Threshold, Function, Walk, Delay *Controlled by PC
Digital QDC	Integral time 8 ns to 4000 ns
Digital PSA	FAST / SLOW
External Input / Output terminal (TTL level)	CLK input, CLK output, GATE input, VETO input, CLR input, OR output (LEMO connector)[*1]
External dimensions Weight	VME1U 20(W) x 262(H) x 187(D), unit: mm About 460g

*Images is for illustration purpose.
*Please note that contents may change without prior notice.

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